[0139] Step 26: S/D Anneal.

[0140] **FIG. 3W** shows the device **60** of **FIG. 3V** after a conventional S/D anneal of the RSD regions **18FIG. 3W** shows the device **60** of **FIG. 3V** after a conventional S/D anneal (preferably RTA, spike or non-melt laser anneal. After this step, one can follow conventional process to finish device (silicidation and making contacts, etc., as will be well understood by those skilled in the art. The recessed channel is located below the gate **32**" in **FIG. 3W** in the SOI silicon **14** between the spacers **34**.

[0141] While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modificawithin the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.

1. A method of forming and FET device with a raised silicon source/drain and a gate electrode structure on an SOI structure comprising an SOI silicon layer formed on a substrate wherein the substrate comprises an insulator by the following steps:

forming a SiGe layer over the silicon layer,

forming a raised source/drain layer over the SiGe layer,

etching through the raised source/drain layer and the SiGe layer to form a gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer thereby forming a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer,

lining the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers,

forming a gate electrode inside the inner sidewall spacers on a cleaned surface of the silicon layer,

forming external sidewall spacers adjacent to the gate electrode between the raised source/drain regions adjacent to the inner sidewall spacers, and

doping the source/drain regions,

whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions above the SiGe layer.

2. The method of claim 1 wherein an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space.

3. The method of claim 1 including the steps of forming the gate electrode space by the steps as follows:

forming a dummy gate over the source/drain layer,

forming a conformal outside spacer layer over the dummy gate,

forming an exterior masking layer over the outside spacer layer,

etching back the exterior masking layer to expose the dummy gate, and

removing the dummy gate to form the gate electrode space.

4. The method of claim 3 wherein the exterior masking layer is composed of silicon dioxide which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof.

5. The method of claim 3 wherein

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer.

6. The method of claim 2 including the steps of forming the gate electrode space by the steps as follows:

forming a dummy gate over the source/drain layer,

forming a conformal outside spacer layer over the dummy gate,

forming an exterior masking layer over the outside spacer layer,

etching back the exterior masking layer to expose the dummy gate, and

removing the dummy gate to form the gate electrode space.

7. The method of claim 1 wherein:

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space; and

forming the gate electrode space by forming a dummy gate over the source/drain layer, forming a conformal outside spacer layer over the dummy gate, forming an exterior masking layer over the outside spacer layer,

etching back the exterior masking layer to expose the dummy gate, and removing the dummy gate to form the gate electrode space.

8. The method of claim 1 wherein the insulator forming the substrate comprises silicon oxide.

9. The method of claim 3 wherein

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer.

10. The method of claim 3 wherein

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space,

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer, and